

IMAGE SENSOR LAB ISL- 4800™

Product Specification

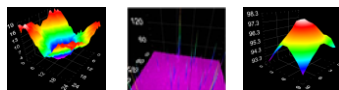
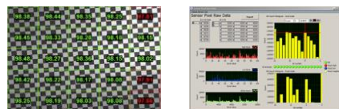
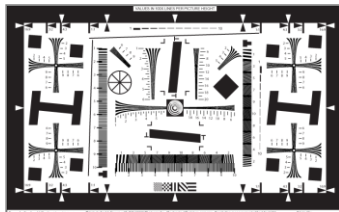


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1. INTRODUCTION

The ISL-4800™ is a cost-effective combination of sensor interface, test electronics, and application software that provides complete communications, image capture, and characterization testing, of a wide variety of image sensors. The ISL-4800 supports both bit-parallel output type, and high-speed serial (including MIPI and SMIA) output type image sensors. The ISL software application offers scripting and plug-in functionality, allowing enhanced graphical user interfaces to specific image sensor models as well as customized image processing analysis and characterization testing routines.

The ISL software application is pre-configured with a library of testing and characterization routines, as well as many of the processing tools that are typically needed for thorough evaluation and testing of image sensors.

2. CONTACT INFORMATION

The primary contact for information regarding sales, support, and technical information is:

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<http://www.jovasolutions.com>

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3.2 REFERENCED DOCUMENTS

Here are documents related to the ISL-4800, which you may find useful:

Description	Doc. No	Company/Author	Rev. Date
ISL-4800 Product Specification	210-4800-01	Jova Solutions	03/28/2010
ISL Basic User Manual	210-0001-07	Jova Solutions	07/14/2009
ISL Advanced Analysis Guide	210-0002-08	Jova Solutions	07/14/2009
ISL Quick Start Guide	210-0008-02	Jova Solutions	07/14/2009
ISL Test and Automation Suite Guide	210-0003-05	Jova Solutions	07/14/2009

4. HARDWARE FUNCTIONAL DESCRIPTION

4.1 OVERVIEW

The Image Sensor Lab ISL-4800 is an electronic image sensor interface with built-in test and measurement capabilities. The ISL-4800 is a mixed signal device and includes programmable power supplies and oscillator, a flexible sensor image data frame capture capability. I2C, SPI, and UART sensor communication channels are also supplied.

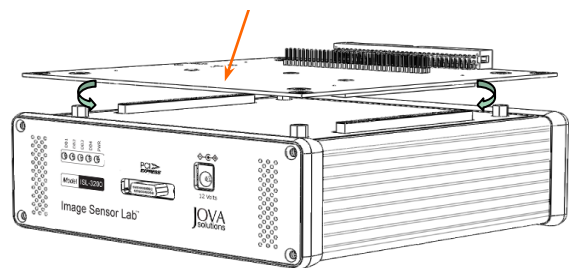
- External 4-lane PCIe interface (10 Gbps)
- Programmable power supplies with voltage and current measurement
- Programmable master clock oscillator up to 136 MHz, FPGA clock to 800 MHz
- 8 and 16 bit data bit-parallel capture into on-board memory
- High-Speed serial sensor interface (2/4 lane MIPI, SMIA, LVDS)
- 256 Mbytes on-board memory (2.6 Gbytes/sec bandwidth)
- 24 additional LVDS-pairs or 50 Digital I/O
- I2C, SPI, and UART sensor communications provided
- Sensor signal voltage translation buffers with programmable isolation
- Built-in timer/counter
- Optional embedded Volt-Ohm Meter with 2 by 64 switch matrix (Short/Open test capable)
- Drivers and automation API available

Image Sensors are typically connected to the ISL-4800 by a custom adapter board, which is mounted to the top of the ISL-4800, using the two 160-pin high density connectors, as shown in the figure below.

160-pin High-density Connectors

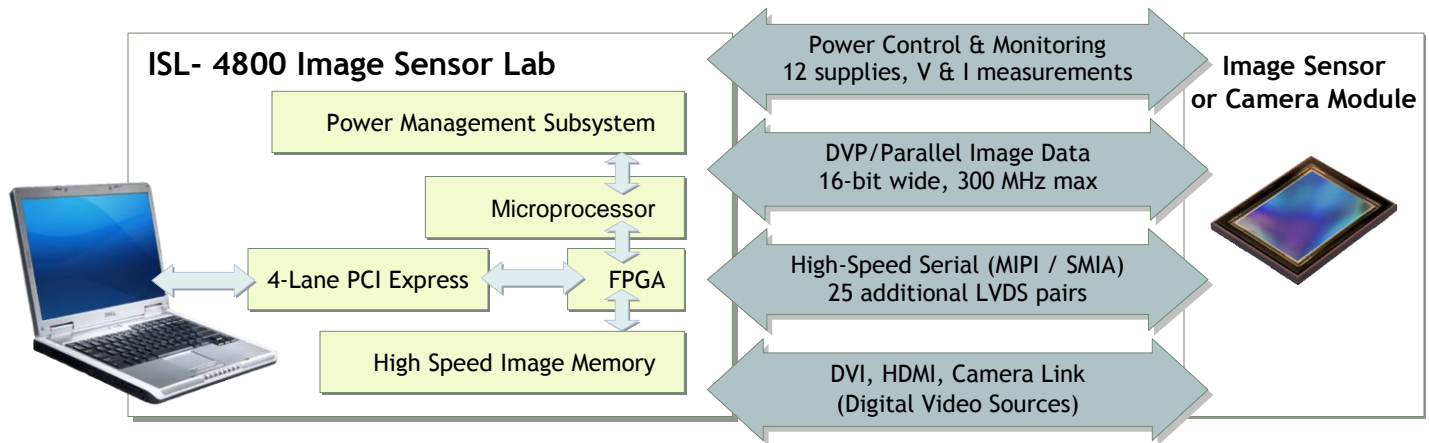


Customer-specific Adapter Board



The ISL-4800 is housed in a compact 160 mm x 240 mm x 53 mm enclosure that is connected to the host computer via an external PCIe cable.

A block diagram showing the major components of the ISL-4800 is shown below. The image sensor is connected to internal circuitry through voltage level translation buffers in order to accommodate image sensors operating with different signal levels. An FPGA is used for the frame capture logic as well as the built-in timer/counter measurements. A microcontroller is also used within the ISL-4800 to control and coordinate the various devices, including the power management circuitry. Twelve power supplies are included, with voltage and current measurement capability. A high-resolution current measurement mode is available for measuring stand-by currents in the μA range.



4.2 HARDWARE CONFIGURATION OPTIONS

The ISL-4800 is offered with two hardware-configuration options that are summarized in the table below.

Option	Description
VOM	<p>The VOM option adds Voltage and Resistance measurement capabilities in two instrument modes to support unpowered shorts/opens testing and signal voltage monitoring during powered testing.</p> <p>The DMM mode provides approximately 4-digit measurement resolution at sampling rates in the 1K-10K samples per second range.</p> <p>The VOM mode provides approximately 7-digit measurement resolution at sampling rates between 10-100 samples per second.</p> <p>The instrumentation is connected to various interface signals through an Analog Switch matrix in a 2 x 64 cross-point configuration (HI and LO probe vs. 64 test points).</p>

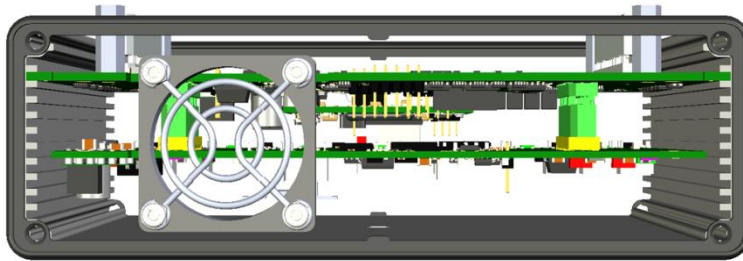
4.3 PHYSICAL DESCRIPTION

The ISL-4800 instrument is housed in a metal enclosure with connectors for power, communications, and image sensor connection. The overall size is 160mm wide by 240mm deep by 51mm high.

Two 160-pin high-density connectors on the top of the ISL-4800 are used for sensor power and interface signals.

The ISL-4800 is powered from an external +12VDC, 5 Amp maximum power source, via a 2.5mm center pin Power Plug (e.g., a 12V laptop style supply).

The ISL-4800 is controlled via an external PCIe high-speed interface.



4.4 TEST INTERFACE

The ISL-4800 Series Test Interface connections are detailed in the diagrams below.

J1			West
Signal	Pin	Pin	Signal
GND	2	1	GND
PSB_OUT	4	3	
PSB_RTN	6	5	
	8	7	ADPT_3V2_OUT
	10	9	ADPT_3V2_GND
PSD_OUT	12	11	PSF_OUT
PSD_RTN	14	13	PSF_RTN
	16	15	
	18	17	
GND	20	19	GND
LED_PWM2_OUT	22	21	PSH_OUT
LED_PWM2_RTN	24	23	PSH_RTN
BRITE_LED2_OUT	26	25	
BRITE_LED2_RTN	28	27	
	30	29	
RGB2_OUT	32	31	PWM2_OUT
RGB2_RED_RTN	34	33	PWM2_RTN
RGB2_GRN_RTN	36	35	PSY_OUT
RGB2_BLU_RTN	38	37	PSY_RTN
GND	40	39	GND
GND	42	41	GND
PSU_OUT	44	43	I2C_VREF
PSU_RTN	46	45	I2C_SCL_RES
PSU_OUT_Sense	48	47	I2C_SDA_RES
PSU_RTN_Sense	50	49	I2C_SCL
ABS_USER0	52	51	I2C_SDA
ABS_USER1	54	53	ADPT_I2C_SDA
ABS_USER2	56	55	ADPT_I2C_SCL
ABS_USER3	58	57	ADPT_I2C_VREF
GND	60	59	GND
ABS_PSU_OUT	62	61	REFCLK
ABS_PSU_RTN	64	63	PIXCLK
	66	65	PSIO
	68	67	
	70	69	
FPGA Jumper	72	71	UART_TX
+3.3V	74	73	UART_RX
LVDS Choice	76	75	UART_RTS
+2.5V_LDO	78	77	UART_CTS
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

J2			East
Signal	Pin	Pin	Signal
GND	2	1	GND
PSIO	4	3	PSA_OUT
PSIO	6	5	PSA_RTN
ADPT_3V1_OUT	8	7	
ADPT_3V1_GND	10	9	
PSE_OUT**	12	11	PSC_OUT
PSE_RTN**	14	13	PSC_RTN
	16	15	
	18	17	
GND	20	19	GND
PSG_OUT	22	21	LED_PWM1_OUT
PSG_RTN	24	23	LED_PWM1_RTN
	26	25	BRITE_LED1_OUT
	28	27	BRITE_LED1_RTN
	30	29	
PWM1_OUT	32	31	RGB1_OUT
PWM1_RTN	34	33	RGB1_RED_RTN
PSX_OUT	36	35	RGB1_GRN_RTN
PSX_RTN	38	37	RGB1_BLU_RTN
GND	40	39	GND
GND	42	41	GND
SPI_SCK	44	43	
SPI_SDO	46	45	
SPI_SDI	48	47	
SPI_nSS	50	49	
SPI_nCS0	52	51	
SPI_nCS1	54	53	
SPI_nCS2	56	55	
SPI_nCS3	58	57	
GND	60	59	GND
	62	61	
ADPT_SPI_nCS0	64	63	
ADPT_SPI_nCS1	66	65	
ADPT_SPI_nCS2	68	67	
ADPT_SPI_nCS3	70	69	
ADPT_SPI_nCS4	72	71	ADPT_SPI_nSS
ADPT_SPI_nCS5	74	73	ADPT_SPI_SDI
ADPT_SPI_nCS6	76	75	ADPT_SPI_SCK
ADPT_SPI_nCS7	78	77	ADPT_SPI_SDO
GND	80	79	GND
Continued			Pins 81 through 160 Next Page

Notes: Gray - Reserved for future use. Do not connect to these pins.

Yellow - Analog boundary scan test point.

** PSE of the ISL-4800 is of a different range than in the ISL-1600

J1 Cont.			West
Signal	Pin	Pin	Signal
GND	82	81	GND
IO_L00_18_P	84	83	DIO_B0 (<i>BOU</i> T-0)
IO_L00_18_N	86	85	DIO_B1 (<i>BOU</i> T-1)
GND	88	87	DIO_B2 (<i>BOU</i> T-2)
IO_L06_18_P	90	89	DIO_B3 (<i>BOU</i> T-3)
IO_L06_18_N	92	91	DIO_B4 (<i>BIN</i> -0)
GND	94	93	DIO_B5 (<i>BIN</i> -1)
IO_L02_18_P	96	95	DIO_B6 (<i>BIN</i> -2)
IO_L02_18_N	98	97	DIO_B7 (<i>BIN</i> -3)
GND	100	99	GND
GND	102	101	
IO_L04_18_P	104	103	DIO_D0 (<i>D</i> 0)
IO_L04_18_N	106	105	DIO_D1 (<i>D</i> 1)
GND	108	107	DIO_D2 (<i>D</i> 2)
IO_L08_18_P	110	109	DIO_D3 (<i>D</i> 3)
IO_L08_18_N	112	111	DIO_D4 (<i>D</i> 4)
GND	114	113	DIO_D5 (<i>D</i> 5)
IO_L11_18_P	116	115	DIO_D6 (<i>D</i> 6)
IO_L11_18_N	118	117	DIO_D7 (<i>D</i> 7)
GND	120	119	GND
GND	122	121	GND
IO_L13_18_P	124	123	IO_L15_18_P
IO_L13_18_N	126	125	IO_L15_18_N
GND	128	127	GND
IO_L03_18_P	130	129	IO_L17_18_P
IO_L03_18_N	132	131	IO_L17_18_N
GND	134	133	GND
IO_L07_18_P	136	135	IO_L16_18_P
IO_L07_18_N	138	137	IO_L16_18_N
GND	140	139	GND
GND	142	141	GND
IO_L09_18_P	144	143	IO_L14_18_P
IO_L09_18_N	146	145	IO_L14_18_N
GND	148	147	GND
IO_L19_18_P	150	149	IO_L18_18_P
IO_L19_18_N	152	151	IO_L18_18_N
GND	154	153	GND
IO_L05_18_P	156	155	IO_L10_18_P
IO_L05_18_N	158	157	IO_L10_18_N
GND	160	159	GND

J2 Cont.			East
Signal	Pin	Pin	Signal
GND	82	81	GND
DIO_A0 (<i>V</i> SYN <i>C</i>)	84	83	
DIO_A1 (<i>X</i> SYN <i>C</i> -0)	86	85	
DIO_A2 (<i>X</i> SYN <i>C</i> -1)	88	87	
DIO_A3 (<i>X</i> SYN <i>C</i> -2)	90	89	
DIO_A4 (<i>H</i> I-Z)	92	91	
DIO_A5 (<i>H</i> I-Z)	94	93	
DIO_A6 (<i>H</i> I-Z)	96	95	
DIO_A7 (<i>H</i> I-Z)	98	97	
GND	100	99	GND
GND	102	101	
DIO_C0 (<i>D</i> 8)	104	103	
DIO_C1 (<i>D</i> 9)	106	105	
DIO_C2 (<i>D</i> 10)	108	107	
DIO_C3 (<i>D</i> 11)	110	109	
DIO_C4 (<i>D</i> 12)	112	111	
DIO_C5 (<i>D</i> 13)	114	113	
DIO_C6 (<i>D</i> 14)	116	115	
DIO_C7 (<i>D</i> 15)	118	117	
GND	120	119	GND
GND	122	121	GND
IO_L8_16_P	124	123	IO_L5_16_P
IO_L8_16_N	126	125	IO_L5_16_N
GND	128	127	GND
MIPI_HS_CLK_P	130	129	IO_L6_16_P
MIPI_HS_CLK_N	132	131	IO_L6_16_N
GND	134	133	GND
MIPI_HS_D1_P	136	135	IO_L7_16_P
MIPI_HS_D1_N	138	137	IO_L7_16_N
GND	140	139	GND
GND	142	141	GND
MIPI_HS_D2_P	144	143	IO_L9_16_P
MIPI_HS_D2_N	146	145	IO_L9_16_N
GND	148	147	GND
MIPI_HS_D3_P	150	149	IO_L12_16_P
MIPI_HS_D3_N	152	151	IO_L12_16_N
GND	154	153	GND
MIPI_HS_D4_P	156	155	IO_L16_16_P
MIPI_HS_D4_N	158	157	IO_L16_16_N
GND	160	159	GND

Notes: Gray - Reserved for Future Use. Do Not Connect to these pins.

Yellow - Analog boundary scan test point.

ISL-1600 Compatibility Signals shown in (*Parentheses and Italic*)

4.4.1 ISL-4800 vs. ISL-3200 & ISL-1600 Compatibility Considerations

ISL-3200 and ISL-4800 power supplies PSA through PSD are similar in effective operating voltage range to an ISL-1600 PS01 model supply (0-5V 200uA).

In the ISL-1600, PSE, a PS01 type supply provides its output power to internal buffer circuitry as well, as being available for external use. In the ISL-3200 and ISL-4800, a separate PSIO supply provides power to internal buffers and is available as a voltage reference at the test interface. Other supplies that meet or exceed the PS01 type supply performance for most applications are available for use to provide PSE power.

The ISL-1600-PS03 type supply has been incorporated and is available as PSU.

To minimize ISL-1600 user efforts to transition to an ISL-3200 or ISL-4800 Series unit, an FPGA logic file is provided for use containing the ISL-1600 Capture Logic. The use of certain ISL-3200 signals are either fixed or prohibited.

4.5 HOST COMPUTER INTERFACE

4.5.1 PCIe Interface

The standard host computer interface of the ISL-4800 is a 4-lane PCI Express (PCIe) interface and can be connected to a single lane, dual lane, or quad lane PCIe slot in the host PC.

The PCIe interface uses a standard Molex 74150-0001 connector, which can be connected to the External PCIe connectors that are provided on most laptop computers. An inexpensive simple PCIe plug-in card is also available for desktop and workstation computers.

The ISL-4800 is “GEN2” compliant and will support the 2X speed increase over the current GEN1 speeds.

5. HARDWARE SPECIFICATIONS

5.1 INPUT POWER REQUIREMENTS

The ISL-4800 requires an external power source of +12V, 3 amps minimum.

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Voltage		11.5	12.0	12.5	VDC	
Current		3.0	4.0	5.0	A	
Ripple and Noise				1%	V (p-p)	
Load Regulation			5		%	
Line Regulation			5		%	

External Power Supply

Example AC/DC Adaptors

SL Power Electronics (Ault)	PW153KB1203F01	for 3.4A
	PW174KB1203F01	for 5.0A, recommended

5.2 OUTPUT POWER SPECIFICATION

5.2.1 Output Power Overview

Primary power for the Camera/Sensor and supporting Adaptor circuitry available are dependent on the presence of the optional Power Management Bundle and are detailed in the table below.

Name	Voltage	Current	Remote V-Sense	Analog Scan	CTRL Scan	Low Current	PS Type Source
PSIO	Off/1.25 - 4V 128-steps	100mA	(1)		Yes <i>V only</i>		LDO35
PS-A	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-B	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-C	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-D	Off/1.25 - 4V 128-steps	100mA	n/a (2)	Yes	Yes	Yes	LDO35
PS-E	Off/0.6 - 1.8V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM1
PS-F	Off/0.6 - 1.8V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM1
PS-G	Off/1.2 - 3.4V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM2
PS-H	Off/1.2 - 3.4V 31-steps	600mA	n/a (2)	Yes	Yes	Yes	SM2
PS-U	0-10V 4096-steps	0-TBD (600) mA Current Limit TBD-steps	Yes	Yes(3)	Yes	n/a(4)	Custom
PS-X	Off/1.25 - 3.3V 8 fixed steps	150mA					LDO12
PS-Y	Off/1.25 - 3.3V 8 fixed steps	150mA					LDO12
PS-ADPT-1	Off/3.3V	150mA					LDO0
PS-ADPT-2	Off/3.3V	150mA					LDO0
PWM1	Open Drain	150mA					PWM
PWM2	Open Drain	150mA					PWM
LED-PWM1	Open Drain	150mA					LED-PWM
LED-PWM2	Open Drain	150mA					LED-PWM
BRITE-LED1	29V max	500mA max					SM3
BRITE-LED2	29V max	500mA max					SM3
RGB-LED1 (3 output)	Open Drain	16.6mA					RGB-LED
RGB-LED2 (3 output)	Open Drain	16.6mA					RGB-LED

Notes:

- (1) Capability Not Available
- (2) Capability Not Currently Available -Signal Paths Reserved for Future Possible Upgrade
- (3) PSU Analog Scan Option for Resistance Only - (see separate section)
- (4) PSU Low Current Not Available -- Future Possible Capability

5.2.2 PSIO, PSA, PSB, PSC, PSD (1.25V - 3.8V, 100 mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sensing, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sensing, are supported.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(LDO35)}$ Quiescent current, only one of LDO3, LDO4, LDO5 is enabled	$I_{Q(LDO35)} = I(VIN_LDO35)$		70		μA
$I_{O(LDO35)}$ Output current range				100	mA
$V_{O(LDO35)}$ LDO3, LDO4, LDO5 output voltage	Output Voltage, Selectable via I ² C	Available output voltages : $V_{O(LDO35)TYP} = 1.224 V$ to 4.46 V, 25 mV steps			V
	Dropout voltage, 100-mA load			240	mV
	Total accuracy, 100 mA load $V(VIN_LDO35) = 5 V$	-3%		3%	
	Load regulation, $V(VIN_LDO35) > V_{O(LDO35)TYP} + 0.5 V$ load: 1 mA \rightarrow 50 mA	-1%		1%	
	Line regulation, 10 mA load, $V(VIN_LDO35): V_{O(LDO35)TYP} + 0.5 V \rightarrow 4.7 V$	-1%		1%	
$I_{SC(LDO35)}$ Short circuit current limit	Output grounded		250		mA
$PSR_{f(LDO35)}$ PSRR at 10 kHz	$V(VIN_LDO35) > V_{O(LDO35)} + 1 V$, 50 mA load at output		40		dB
$R_{OCH(LDO35)}$ Discharge resistor	LDO is disabled by I ² C command		400		Ω
$I_{LKG(LDO35)}$ Leakage current	LDO off		1		μA

Note: For proper digital signal operation, both PSIO and PS wired for powering camera/sensor digital IO should be programmed to output the same voltage levels.

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect (excluding PSIO).

5.2.3 PSE, PSF (0.6V - 1.8V, 600mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(SM1)}$	Quiescent current for SM1	$I_{Q(SM1)} = I(VIN_SM1)$, no output load	Not switching		10		μA
		SM1 OFF, set via I ² C			0.1		
$I_{O(SM1)}$	Output current range				600		mA
$V_{O(SM1)}$	Output voltage, PWM mode	Output voltage, selectable via I ² C, Standby OFF		Available output voltages: $V_{O(SM1)TYP} = 0.6V$ to $1.8V$, adjustable in 40 mV steps			V
		$V_{O(SM1)} = V_{SBY(SM1)}$, Output voltage range, Standby ON		Available output voltages: $V_{SBY(SM1)} = 0.6V$ to $1.8V$, adjustable in 40 mV steps			
		Total accuracy, $V_{O(SM1)TYP} = V_{SBY(SM1)} = 1.24V$, $V(VIN_SM1) = 3.0V$ to $4.7V$; $0mA \leq I_{O(SM1)} \leq 600mA$		-3%		3%	
		Line Regulation, $V(VIN_SM1): 3.0 \rightarrow 4.7V$, $I_{O(SM1)} = 10mA$			0.027		%/V
		Load Regulation, $V(VIN_SM1) = 4.7V$, $I_{O(SM1)}: 60mA \rightarrow 540mA$			0.139		%/A
$R_{DS(on)(PSM1)}$	P-channel MOSFET on-resistance	$V(VIN_SM1) = 3.6V$, 100% duty cycle set			310	500	m Ω
$I_{LKG(PSM1)}$	P-channel leakage current				0.1		μA
$R_{DS(on)(NSM1)}$	N-channel MOSFET on-resistance	$V(VIN_SM1) = 3.6V$, 0% duty cycle set			220	330	m Ω
$I_{LKG(NSM1)}$	N-channel leakage current				5		μA
$I_{LIM(SM1)}$	P&N -channel current limit	$3.0V < V(VIN_SM1) < 4.7V$		900	1050	1200	mA
$f_{S(SM1)}$	Oscillator frequency	PWM mode set		1.3	1.5	1.7	MHz
$EFF_{(SM1)}$	Efficiency	$V(VIN_SM1) = 4.2V$, PWM mode, $I_{O(SM1)} = 300mA$, $V_{O(SM1)} = 3V$			90%		
$t_{SS(SM1)}$	Soft start ramp time	Converter OFF \rightarrow ON, $V_{O(SM1)}: 5\% \rightarrow 95\%$ of target value			750		μs
$t_{DLY(SM1)}$	Converter turn-on delay	GPIO1 pin programmed as SM1 converter enable control. Measured from $V(GPIO1): LO \rightarrow HI$			170		μs

A mechanical relay, 50m OHMS max, is used for the output connect/disconnect.

5.2.4 PSG, PSH (1.0V - 3.4V, 600mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
I _{Q(SM2)}	Quiescent current for SM2	I _{Q(SM2)} = I(VIN_ SM2), no output load	Not switching	10			μA	
		SM2 OFF, set via I ² C		0.1				
I _{O(SM2)}	Output current range				600			mA
V _{O(SM2)}	Output voltage	Output voltage , selectable via I ² C, Standby OFF		Available output voltages: V _{O(SM2)TYP} = 1.0 V to 3.4 V, adjustable in 80 mV steps			V	
		V _{O(SM2)} = V _{SBY(SM2)} , Output voltage range, Standby ON		Available output voltages: V _{SBY(SM2)} = 1.0 V to 3.4 V, adjustable in 80 mV steps				
		Total accuracy, V _{O(SM2)TYP} = V _{SM2(SBY)} = 1.8 V, V(VIN_ SM2) = greater of [3.0 V or (V _{O(SM2)} + 0.3 V)] to 4.7 V; 0 mA ≤ I _{O(SM2)} ≤ 600 mA		-3%			3%	
		Line regulation, V(VIN_ SM2) = greater of [3.0 V or (V _{O(SM2)} + 0.3 V)] to 4.7 V; 0 mA ≤ I _{O(SM2)} ≤ 600 mA		0.027			%/V	
		Load regulation, V(VIN_ SM2) = 4.7 V, I _{O(SM2)} : 60 mA → 540 mA		0.139			%/A	
R _{DS(ON)(PSM2)}	P-channel MOSFET on-resistance	V(VIN_ SM2) = 3.6 V, 100% duty cycle set			310	500	mΩ	
I _{LKG(PSM2)}	P-channel leakage current				0.1		μA	
R _{DS(ON)(NSM2)}	N-channel MOSFET on-resistance	V(VIN_ SM2) = 3.6 V, 0% duty cycle set			220	330	mΩ	
I _{LKG(NSM2)}	N-channel leakage current				5		μA	
I _{LIM(SM2)}	P&N -channel current limit	3.0 V < V(VIN_ SM2) < 4.7 V			900	1050 1200	mA	
f _{S(SM2)}	Oscillator frequency	PWM mode set			1.3	1.5 1.7	MHz	
EFF _(SM2)	Efficiency	V(VIN_ SM2) = 4.2 V, I _{O(SM2)} = 300 mA, V _{O(SM2)} = 3 V			90%			
t _{SS(SM2)}	Soft start ramp time	Converter OFF→ON, V _{O(SM2)} : 5% → 95% of target value			750		μs	
t _{DLY(SM2)}	Converter turn-on delay	GPIO2 pin programmed as SM2 converter enable control. Measured from V(GPIO2): LO → HI			170		μs	

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect.

5.2.5 PSU (0V - 10V, 500mA)

- High-resolution low-frequency measurements of output voltage and current, and remote voltage sense, are supported.
- Medium-resolution medium-frequency measurements of output voltage and current, and remote voltage sense, are supported.

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Voltage		0	3-5	10.25 TBD	VDC	Regulated
Current		0		500	mA	Limited
Ripple and Noise						
Voltage			250	500	uVp-p	
			50	100	uVrms	
Current			400	800	nArms	
Load Regulation			TBD			
Transient Response			TBD			
Voltage Programming						
Accuracy			+/- 2.0	+/- 5.0	mV	
Current Limit Programming						
Accuracy			100		uA	
Voltage Measurement						
Accuracy				+/- 6.0	mV	
Current Measurement						
Accuracy			+/- 50		uA	
Fixed Offset		0		100	uA	

A mechanical relay, 50mOHMS max, is used for the output connect/disconnect.

This supply is similar in design to the ISL-1600 power supply model PS03.

Remote regulation voltage sense is available.

Note: The output voltage range of PSU exceeds the range of the VOM circuit during power-on and therefore cannot be directly measured through the Analog Switch Matrix with the VOM option.

5.2.6 PSX, PXY (1.224V - 3.3V, 150 mA)

- Voltage and Current Measurements are not supported.
- Output is not calibrated.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{Q(LDO1,2)}	Quiescent current, either LDO1 or LDO2 enabled, LDO0 disabled	I _{Q(LDO1,2)} = I(VIN_LDO02)	I _{L(LDO1,2)} = −1 mA		15		μA
			I _{L(LDO1,2)} = −150 mA		160		
I _{O(LDO1,2)}	Output current range					150	mA
V _{O(LDO1,2)}	LDO1, LDO2 Output Voltage	Output Voltage, Selectable via I ² C.			Available output voltages: V _{O(LDO1,2)} TYP = 1.25, 1.5, 1.8, 2.5, 2.85, 3, 3.2, 3.3		V
		Dropout voltage, 150 mA load				300	mV
		Total accuracy, V(VIN_LDO02) = 3.65 V		−3%		3%	
		Line Regulation, 100 mA load, V(VIN_LDO02): V _(LDO1,2) TYP + 0.5 V → 4.7 V		−1%		1%	
		Load regulation, load: 10 mA → 150 mA V(VIN_LDO02) > V _{O(LDO1,2)} TYP + 0.5V		−1.5%		1.5%	
PSR(LDO1,2)	PSRR at 20 kHz	150mA load at output, V(VIN_LDO02) − V _{O(LDO1,2)} =1V			40		dB
I _{SC(LDO1,2)}	LDO1&2 short circuit current limit	Output grounded			300		mA
R _{DCH(LDO1,2)}	Discharge resistor	LDO disabled by I ² C command			300		Ω
I _{LKG(LDO1,2)}	Leakage current	LDO off			2		μA

5.2.7 Adaptor Power Output 1 & 2 (+3.3V)

- Voltage and Current Measurements are not supported.
- Output is not calibrated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(LDO0)}$	Quiescent current	Internally connected to VIN_LDO12 pin	$I(LDO0) = -1 \text{ mA}$		15	μA
			$I(LDO0) = -150 \text{ mA}$		160	
$I_{O(LDO0)}$	Output current range				150	mA
$V_{O(LDO0)}$	Output voltage	Fixed output voltage value		3.3		V
		Dropout voltage, $I(LDO0) = -150 \text{ mA}$			300	mV
		Total accuracy	-3%		3%	
		Line regulation, $V(OUT): V_{O(LDO0)} + 0.5 \rightarrow 4.7 \text{ V}$, $I(LDO0) = -100 \text{ mA}$	-1%		1%	
		Load regulation, $I(LDO0) = -10 \text{ mA} \rightarrow -150 \text{ mA}$	-1.5%		1.5%	
$PSR_{(LDO0)}$	PSRR at 20 kHz	150 mA load at output, $V(VIN_LDO12) - V_{O(LDO1,2)} = 1 \text{ V}$		40		dB
$I_{SC(LDO0)}$	Short circuit current limit	$V(LDO0) = 0 \text{ V}$		300		mA
$I_{LKG(LDO0)}$	Leakage current	LDO off		1		μA

5.2.8 PWM Open Drain Outputs 1 & 2

PWM DRIVER , PWM OPEN DRAIN OUTPUT				
V _{OL(PWM)}	Low level output voltage	I(PWM)= 150 mA	0.5	V
F _{PWM}	PWM driver frequency	Frequency range	Set via I ² C, F _{PWM} = 0.5/1/1.5/2/3/4.5/7.8/15.6	
		Total accuracy, relative to selected value	-20%	+20%
D _{PWM}	PWM driver duty cycle	Duty cycle range	D _{PWM} = 6.25% to 100%, set via I ² C, 6.25% minimum step	

5.2.9 LED PWM Open Drain Outputs 1 & 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT								
D _{LEDPWM}	LED_PWM driver duty cycle	Duty cycle range		D _{LEDPWM} = 0% to 99.6%, set via I ² C, 256 steps 0.4% minimum step				
F _{REP(LED PWM)}	LED_PWM driver duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0	122			Hz	
			SM3_LF_OSC = 1	180				
V _{OL(LED PWM)}	Low level output voltage	I(LED_PWM) = 150 mA			0.5			V
V _{OH(LED PWM)}	High level output voltage				6			V

5.2.10 RGB LED Open Drain Outputs 1 & 2

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS							
t _{FLASH(RGB)}	Flashing period	Flashing period range		t _{FLASH(RGB)} = 1 to 8 sec, set via I ² C, 0.5 sec minimum step, 8 steps			sec
		Total accuracy		-20% +20%			
t _{FLASH(ON)}	Flash on time	Flash on time range, value selectable by I ² C		Set via I ² C , t _{FLASH(ON)} = 0.1/0.15/0.2/0.25/0.3/0.4/0.5/0.6 Sec			sec
		Total accuracy, relative to selected value		-20% +20%			
D _{RGB}	Duty cycle	Duty cycle range, value selectable via I ² C		D _{RGB} = 0% to 99.98%, set via I ² C, 3.23% minimum step			
I _{SINK(RGB)}	RGB output sink current	V(RED) = V(GREEN) = V(BLUE) = 2 V, set via I2C RGB_ISET1,0	00 = (Driver set to OFF)				mA
			01 =	2.4	4	5.6	
			10 =	4.8	8	11.2	
			11 =	7	12	16.6	
V _{OL(RGB)}	Low level output voltage	Output low voltage, 8 mA load, RED/GREEN/BLUE PINS		0.3			V
I _{LKG(RGB)}	Output off leakage current	V(RED)=V(GREEN)=V(BLUE) = 4.7 V, all drivers disabled		1			μA

5.2.11 Bright White LED Driver Outputs 1 & 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WHITE LED CONSTANT CURRENT DRIVER						
V _{VIN(SM3)}	Input Voltage range	V(OUT) = 3.3 V	3.0		4.7	V
V _{OVP3}	Output over-voltage trip	OVP detected at V(SM3) > V _{OVP3}	26.5	29	30	V
V _{HYS(OVP3)}	Output over-voltage hysteresis	OVP not detected at V(SM3) < V _{OVP3} - V _{HYS(OVP3)}		1.8		V
V _{SM3REF}	LED current sense threshold	LED current below regulation point at V(FB3) < V _{SM3REF}	244	252	260	mV
I _{O(SM3)}	LED current	Current range, V _{in} = 3.3 V, $I_{O(SM3)} = \frac{V(SM3REF)}{R_{FB3}}$	0		25	mA
		Total accuracy, I _{O(SM3)} = 10mA	-10%		10%	
D _{SM3SW}	LED switch duty cycle	Duty cycle range	D _{SM3SW} = 0% to 99.6%, set via I ² C, 256 steps, 0.4% minimum step			–
F _{REP_SM3}	LED switch duty cycle pattern repetition rate	256 pulses within repetition rate time	SM3_LF_OSC = 0		122	Hz
			SM3_LF_OSC = 1		183	
R _{DS(on)(SM3SW)}	LED switch MOSFET on-resistance	V(OUT)=3.6 V; I(SM3SW)=20 mA		1	2	Ω
I _{LKG(SM3SW)}	LED switch MOSFET leakage			1		μA
R _{DS(on)(L3)}	Power stage MOSFET on-resistance	V(OUT) = 3.6 V; I(L3) = 200 mA		300	600	mΩ
I _{LKG(L3)}	Power stage MOSFET leakage			1		μA
I _{MAX(L3)}	Power stage MOSFET current limit	3 V < V(OUT) < 4.7 V	400	500	600	mA

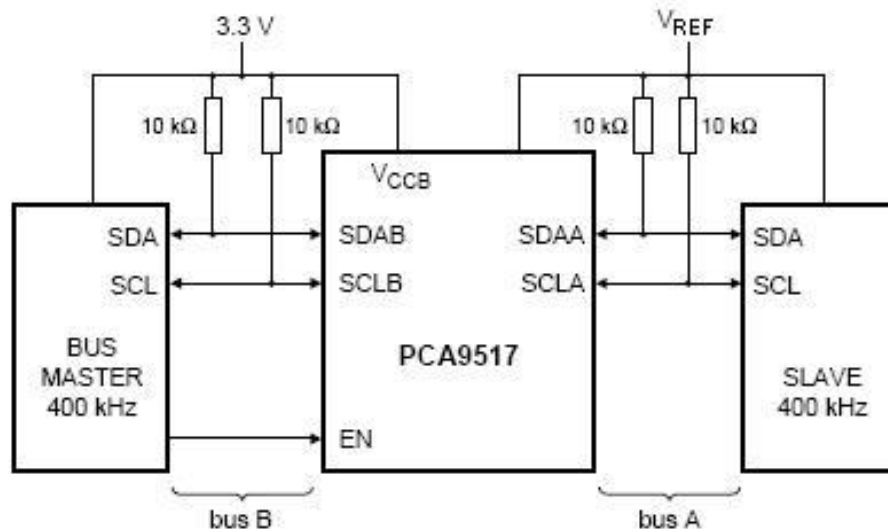
5.3 SENSOR COMMUNICATION

The ISL-4800 on-board processor provides I2C, SPI, and UART I/O to the connectors that can be passed through the adapter board to the image sensor.

5.3.1 I2C Bus Interface

The I2C signals SDA and SCL are bidirectional and open drain. These signals, therefore, require special considerations for signal termination to the digital IO voltage source.

The user must provide pull-up resistors of appropriate value, on the adapter board assembly. The resistors should be placed between the I2C signal pull-up inputs to the ISL-4800 interface and the I2C VCC ref voltage input of the adaptor interface. The PSIO supply, or the desired PSA through PSH supplies, may be tied to the I2C VCC ref input, or other application specific power reference.



5.3.2 SPI Bus Interface

The Serial Peripheral Interface (SPI) sub-system supports full-duplex synchronous serial communications.

Primary features of the SPI sub-system are:

- Separate SPI signal pins for Camera/UUT and Adaptor use
- Camera SPI signal levels are variable with programmed setting of PSIO. (see paragraph 5.4)
- Adaptor SPI signal levels at 3.3v
- Four (4) Camera Chip Select Signals (negative true)
- Eight (8) Adaptor Chip Select Signals (negative true)
- SCK Frequency range, 39.0625 KHz to 20 MHz

5.3.3 UART Interface

The Universal Asynchronous Receiver Transmitter (UART) sub-system supports full-duplex serial communications, and can be configured to support hardware flow control via CTS and RTS signals.

Primary features of the UART sub-system are:

- Full-Duplex 8 or 9-bit transmission through TX and RX signal pins
- Even, Odd or No Parity options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control option with CTS and RTS signal pins
- UART Baud Rate range, 19.0735 bps to 5 Mbps
- Parity, Framing Error Detection
- 1K Byte Receive Buffer
- 3.3V signal level standard, optional open drain with external pull up to 5V

5.4 CLOCKS

The Reference clock (REFCLK) source for the image sensor can come from one of three sources

- an on-board programmable oscillator clock (OSCCLK)
- an FPGA based clock
- an externally provided clock on the adapter circuitry

The Capture Clock (CAPCLK) can be either the Reference clock (REFCLK) going to the image sensor or the Pixel Clock (PIXCLK) coming from the image sensor.

5.4.1 Internal Clock Generation (OSCCLK and REFCLK)

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Oscillator Output Frequency (OSCCLK)		1.039 KHz		68.0254 MHz		OSCCLK
Total Frequency Accuracy			0.5	1.6	%	
Frequency Drift Over Temperature			10		ppm/degree C	
Frequency Drift Over Supply			0.05		%/V	
Long Term Frequency Stability			300		ppm/sqr kHr	
Timing Jitter			1		%	
Duty Cycle		49	50	51	%	
Maximum Useable Frequency				165.2 121.2 63.4	MHz MHz MHz	Design Range 3.3 V Design Range 2.5V Design Range 1.8V

5.4.2 Capture Clock “CAPCLK”

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Clock Input Frequency (PIXCLK or REFCLK) *note additional restriction from FPGA on frequency				165.2 150.3 116.9	MHz MHz MHz	Design Range 3.3 V Design Range 2.5V Design Range 1.8V
Duty Cycle		45	50	55	%	

5.5 PARALLEL IMAGE DATA INTERFACE SPECIFICATION

TBD

5.5.1 Static Digital Input and Output Control

Four (4) general-purpose digital inputs are available at the connector for connection from the image sensor. These lines can be used to receive shutter, LED, Motor or other digital signals from the image sensor. Logic detects and maintains a single change of state for each of these inputs, as well as providing live state status.

Four (4) general-purpose digital outputs are available at the connector for connection to the image sensor. These lines can be control the sensor RESET, CAPTURE or other sensor digital input.

5.5.2 Synchronization Signals

The ISL-4800 provides flexibility to configure the image frame capture logic for operation with most image sensor interface functions. The table below shows the frame capture configuration variables.

Frame Capture Configuration

Configuration Bit	Selection
Capture Clock	REFCLK or PIXCLK
Clock Edge	RISING or FALLING
Vsync Frame Start Edge	RISING or FALLING
Vsync Frame End Edge	RISING or FALLING
Xsync0 Gating	ENABLED or DISABLE
Xsync0 Gating State	HIGH or LOW
Xsync1 Gating	ENABLED or DISABLE
Xsync1 Gating State	HIGH or LOW
Xsync2 Gating	ENABLED or DISABLE
Xsync2 Gating State	HIGH or LOW

5.6 SERIAL IMAGE DATA INTERFACE SPECIFICATION

The ISL-4800 supports multiple high-speed serial interface standards (**MIPI®** and **SMIA**) and provides 25 additional high-speed serial LVDS line pairs that can be used to interface to non-standard high-speed serial interfaces.

The ISL-4800 high-speed serial interface also supports both **DVI** and **HDMI** digital video standards.

5.6.1 MIPI®

MIPI® (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are DPHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.



The ISL-4800 CSI2 Mode functionality includes:

- Configure 1, 2, or 4 data lanes (4-lane MIPI Support requires extra IP license)
- Up to 960 Mbps per lane:
- Interface signals as defined in Appendix B of MIPI® CSI1 specifications;
- Support of all primary data formats, and more

The IP core used in the ISL-4800 has passed the UNH IOL labs interoperability tests and has been qualified to 960 Mbps per data lane.

The hardware supports a single clock lane and up to four data lanes of MIPI compliant LVDS pairs. The FPGA core logic supports only two data lanes by default, with a future option to support four data lanes.

5.6.2 SMIA

SMIA (Standard Mobile Imaging Architecture) is an industry consortium, which defines standards for mobile imager modules. SMIA standards encompass several aspects of the imager, allowing pin level compatibility. One of those standards is CCP2 - high speed communication between the sensor and a host application processor.



The ISL-4800 supports the following CCP2 Mode functionality features:

- Class ,0, 1, and 2
- Up to 650 Mbps
- Supports all data formats as defined in Chapter 5 of the CCP2 Specification
- Receiver behavior as recommended in Chapter 8 of the CCP2 Specifications.

5.6.3 LVDS

A total of twenty-four (24) LVDS pairs are provided in two functional/electrical groups; Bank-16 and Bank-18. Each bank is supported within separate FPGA I/O blocks with separate timing and electrical I/O references.

5.6.3.1 LVDS Bank-16

LVDS Bank-16 provides seven (6) LVDS pairs, or fourteen (12) single-ended signals, or a combination of LVDS and single-ended, with a fixed bank I/O voltage reference of 2.5V and a 100 ohm digitally controlled impedance (programmable). FPGA logic provisioning is optional per custom requirement.

5.6.3.2 LVDS Bank-18

LVDS Bank-18 provides eighteen (18) LVDS pairs, or thirty-six (36) single-ended signals, or a combination of LVDS and single-ended, with a user defined bank I/O voltage reference of 2.5V and a 100 ohm digitally controlled impedance (programmable), 3.3V or other pending user requirements. FPGA logic provisioning is optional per custom requirement.

5.6.4 DVI Video Input

The Digital Visual Interface (DVI) is a video interface standard designed to provide very high visual quality on digital display devices. It was developed by an industry consortium, the Digital Display Working Group (DDWG) to replace the “legacy analog technology” VGA connector standard.



DVI is designed for carrying uncompressed digital video data to a display. A DVI link consists of four twisted pairs of wires (red, green, blue, and clock) to transmit 24 bits per pixel.

5.6.5 HDMI Video Input

HDMI (High-Definition Multimedia Interface) is a compact audio/video interface for transmitting uncompressed digital data. HDMI supports, on a single cable, any TV or PC video format; up to 8 channels of digital audio; and a Consumer Electronics Control (CEC) connection.



The ISL-4800 supports only the digital video portion of the connected HDMI signal.

5.7 MECHANICAL SPECIFICATIONS

5.7.1 Top Down View

TBD

5.7.2 Connector Specifications

5.7.2.1 Input Power Connection

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Size						
Length			240		mm	Excluding optional mounting brackets or feet.
Width			160		mm	
Height			51		mm	
Weight			32		Ounces	

Module input power is provided through a 2.5mm ID, 5.5mm OD, center-pin positive receptacle.

Receptacle: (inside ISL-4800)

CUI, Inc, PN: **PJ-102BH**
 Switchcraft PN: **RAPC712**
 +12VDC Center Pin
 DC Return Outer Ring

Plug: (example for reference only)

CUI Inc. PN: **PP3-002B**
 Switchcraft PN: **760**

5.7.2.2 PCI Express Interface Connection

Receptacle: (inside ISL-4800)

Molex PN: **75586-0011**

5.7.2.3 PCI Express Interface Cable

Molex PN: **74546-0401** 1 meter
 Molex PN: **74546-0403** 3 meter
 Molex PN: **74546-0405** 5 meter

5.7.2.4 PCI Express PC Interface Card

5.7.2.5 USB 3.0 Interface Connection

TBD

5.7.2.6 Sensor Adaptor Interface Connection

The ISL-4800 test interface connector pins are detailed in (paragraph 4.4).

The mating connector (used on the adapter boards) is SAMTEC PN: **QSE-080-01-F-D-A**.

5.8 ENVIRONMENTAL SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
Temperature		0		40	C	
Humidity				TBD	%	Non-Condensing
Altitude				10,000	ft	
Airflow						

6. VOM OPTION

6.1 MEASUREMENT BUS

The 2-Wire VOM option adds analog boundary scan capability with a HI_BUS and LO_BUS and programmable connections, through a 2x64 matrix of analog switches to the sensor signals and measurement instruments. The 2x64 configuration provides 2/4 wire access between instruments and the signals of the device under test.

6.1.1 2-Wire x 64 Analog Switch Matrix

The Analog Devices' ADG791 series device is used for these analog switches.

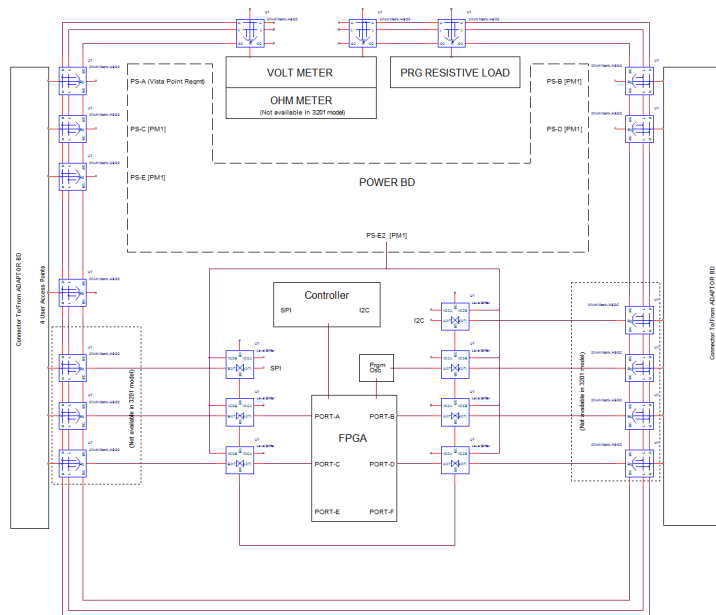
Two instrument-probe-signals, referred to as the HI_Bus and LO_Bus, run the perimeter of the Signal Board.

A series of 1x2 Analog Matrix Switches connect various instrumentation or test signals to either the HI_Bus or LO_Bus lines.

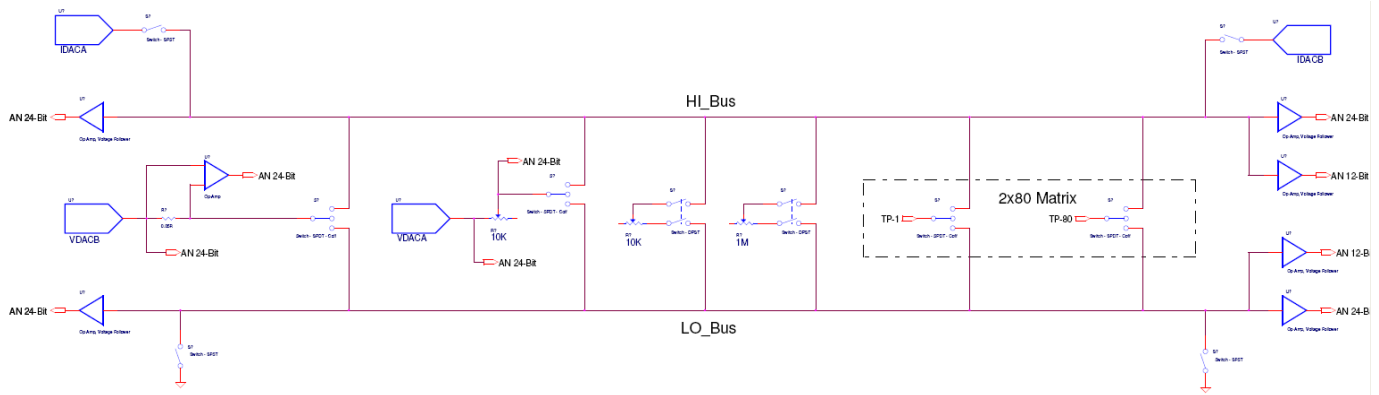
The VOM instrument signals are connected to the HI/LO Buses at each end of the Buses. All other instrumentation or test signals are connected between the ends.

Note: The voltage levels from PS-U exceed the limits of the switch matrix therefore PS-U voltage will be measured separately.

Mechanical relays are used to connect the PS-U to the HI_Bus or LO_Bus during power off ohms measurement (for shorts/opens testing).



6.2 SOURCES AND LOADS



6.2.1 Programmable Pull-Up Resistor Voltage Source - VDACApu

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
VDACA						
Range		0	1.22	3.8	VDC	
Increment			30		mV	
Short-Circuit Current					mA	
Pull-Up						
POR Default		99.0625	5.06k	10.06k	Ohms	
Range			39.0625			
Increment				5	mA	
Current						

6.2.2 Programmable Pull-Up Resistor - 10KPU

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
10K Pull-Up						
POR Default		99.0625	5.06k	10.06k	Ohms	
Range			39.0625			
Increment				5	mA	
Current						

6.2.3 Programmable Voltage Source with Current Measurement - VDACB

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
VDACB						
Range		0	1.22	3.8	VDC	
Increment			30		mV	
Short-Circuit Current					mA	
Current Sense						
Range		1u	100n	30m	A	Minimum target goals
Resolution						

6.2.4 Programmable Current Sources - IDACA & IDACB

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
IDAC Range-1 Range Increment Voltage		2.0833	2.0833	531.25 3.8	uA uA V	Open Circuit
IDAC Range-2 Range Increment Voltage		.004167	4.167	1.0625 3.8	mA uA V	Open Circuit
IDAC Range-3 Range Increment Voltage		.008333	8.333	2.125 3.8	mA uA V	Open Circuit

6.2.5 Programmable Resistive Loads - 10Kohm and 1Mohm

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
10K Load POR Default Range Increment Current		99.0625	5.06k 39.0625	10.06k 5	Ohms mA	
1M Load POR Default Range Increment Current		3.96625k	500.06k 3.90625K	1.0M 500	Ohms uA	

6.3 MEASUREMENTS

6.3.1 Voltage Measurements - 12-bit and 24-bit VADC

Parameter	Symbol	Min	Typical	Max	Unit	Condition/Note
12-Bit VADC						
Range Resolution		0	805	3.8	VDC uV	
Sample Time (1000 points) Sample Time (100 points)				580 80	mSEC	[1]
24-Bit VADC						
Range Resolution		0	596	3.8	VDC nV	
Sample Rate			30	32	Pts/Sec	[2]

Notes:

[1] Based on use of “DMM Measure HL_Bus Voltage.vi” with standard Sample & Hold and Conversion Period settings (as used during product calibration). Faster sample times can be achieved at the expense of less accuracy or increased sample point set noise.

[2] Based on use of standard ADC sampling settings (as used during product calibration). Faster sampling rates can be achieved at the expense of less accuracy or increased sample point set noise.

24-Bit ADC reading are continuously performed in the background and placed into circular storage buffers. Calls to return the contents of the circular buffer can be performed in less than 20ms. Calls to return new samples in the foreground (that is acquiring new samples not placed in the circular buffer) are returned at the sample rate.